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(Received 4 October 1989; accepted 29 October 1989)

Heat treatment at 70 °C of low carrier concentration p -type HgCdTe samples ($p_0 = 8 \times 10^{14} \text{ cm}^{-3}$) generates an inverted surface layer. A two day anneal process below 95 °C did not affect the Hall coefficient, whereas an almost complete recovery was obtained by annealing at 120 °C. While bulk electron mobility, obtained from PEM data, remained high (about $9 \times 10^4 \text{ cm}^2/\text{V s}$ at 77 K), surface mobility is lower by more than an order of magnitude. Surface recombination velocity indicates a continuous improvement with increased temperature, and the activation energy remains equal to the vacancies energy level. The proposed mechanism is that of positive charges in the sulfide migrating towards the interface and generating an image inversion layer.

I. INTRODUCTION

Surface passivations of semiconductor devices are very crucial to the device's performance.¹ Interface properties depend strongly on process parameters. They can result in surface charges, either accumulation or inversion, both undesirable for diodes. Secondly, they set the boundary conditions, as manifested by the surface recombination velocity.² Accordingly, the carrier distribution in the semiconductor is set, and the efficiency as photodevices is determined. The interface properties can be modified by subjecting the device to an annealing process.

Various passivations have been employed with narrow bandgap HgCdTe, including anodic oxide, anodic sulfide, and SiO₂ and ZnS coatings. Recently, we investigated interface properties such as surface recombination velocity, mobility, and carrier concentration.^{3,4} This data was obtained using several opto-galvanomagnetic experiments, including the photoelectromagnetic effect (PEM) for the determination of surface recombination velocity and electron mobility. The properties of anodic sulfide, anodic oxide, and ZnS coatings were compared. Anodic oxide formed an inverted layer on p -type samples, which resembles a two-dimensional layer by virtue of extremely high surface electron mobility.⁴ Both anodic sulfide and ZnS coatings rendered surface recombination with identical activation energies.³ It was concluded that surface traps are related to lattice defects, most probably vacancies. It was also shown that the thickness of the anodic sulfide determines the quality of this passivation. On a carefully prepared sample with a very thin sulfide layer it was possible to obtain a "normal" p -type Hall data even at low temperatures on a sample with acceptor concentration as low as $8 \times 10^{14} \text{ cm}^{-3}$.

In this paper we report a further investigation of the properties of the anodic sulfide interface. Following the formation of an inversion layer, several annealing steps lasting from two hours to two days, were applied. The annealing temperature was gradually increased from 70 to 120 °C. Following each step, full optogalvanomagnetic characterizations were performed.

II. EXPERIMENTAL RESULTS AND DISCUSSION

In order to study the formation and annealing of inversion layers, p -type Hg_{1-x}Cd_xTe samples with composition ratio of $x \sim 0.22$ and with very low carrier concentrations were passivated by anodic sulfide. The low concentration enables the detection of even minute surface charges. A sample with equilibrium concentration of $p_0 = 8 \times 10^{14} \text{ cm}^{-3}$, which previously maintained flatband conditions for three years, was heated to 70 °C in vacuum. After two hours of heating, an inversion layer was formed on its surface. A series of annealing steps were carried out, gradually increasing the annealing temperature. The effect of the annealing process on reducing inversion charges was investigated through the measurement of the Hall coefficient. The experimental results are summarized in Fig. 1. The original measurement shows a classical curve of a p -type sample, with a single sign inversion at about 85 K ("as prepared"). Following the formation of the inverted surface layer, the Hall data renders a typical n -type curve, in which the Hall coefficient remains negative throughout the entire scanned temperature range. Heating for two days at 70 °C did not change the Hall data at all. Similarly, the effect of a two day anneal at 80 °C on the carrier concentrations is hardly noticeable. Only after a two day anneal at 95 °C can an improvement be detected through a narrow region of positive Hall coefficients, before it reverses its sign again. Heating the sample to 120 °C for two days brought about almost a complete recovery of the Hall coefficient. The data at the range of 20–50 K almost coincides with the original bulk measurements, although at lower temperatures a second sign change is still present.

A heat treatment of 70–80 °C generates an electron inversion layer of about $8 \times 10^{11} \text{ cm}^{-2}$. It seems that the positive charges present in the sulfide layer diffuse towards the interface, segregating there, as is frequently the case with defects accumulating at the interface. Consequently, the concentration of negative charges at the surface of the semiconductor increases. Indeed, in samples with a thicker sulfide layer, a higher surface concentration was measured.⁴ Only at higher temperatures, 95 °C and above, does an annealing process

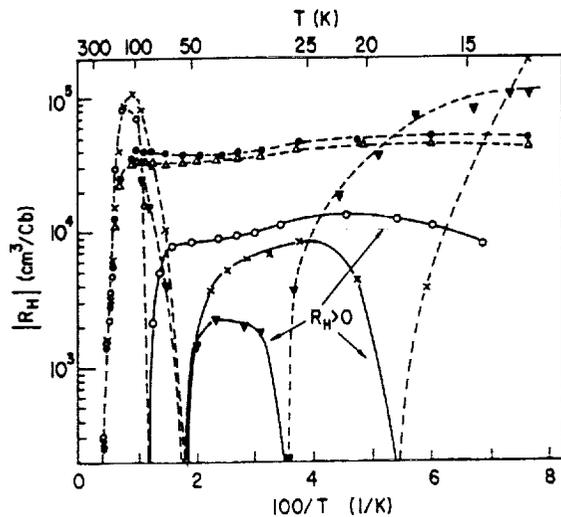


FIG. 1. Hall coefficient of p -HgCdTe, $x = 0.225$, $N_A = 8 \times 10^{14} \text{ cm}^{-3}$, with anodic sulfide. Original well-passivated p -type data ("as prepared"), turns to all negative n -type results following 70°C anneal. Only above 95°C does a positive section reappear, and by 120°C substantial recovery is observed. — $R_H > 0$, --- $R_H < 0$; \circ as prepared, \bullet anneal, 70°C , Δ 2 days, 80°C , ∇ 2 days, 95°C , and \times 2 days, 120°C .

start to take place, reducing the concentration of these charges.

The second basic parameter investigated is the electron mobility. Both Hall and PEM experiments were employed. The bulk electron mobility was extracted from fitting the measured PEM current and from the high temperature Hall data. When an extensive inversion layer is present, the Hall experiment provides information about this layer only. Therefore, the Hall mobility extracted from these samples is

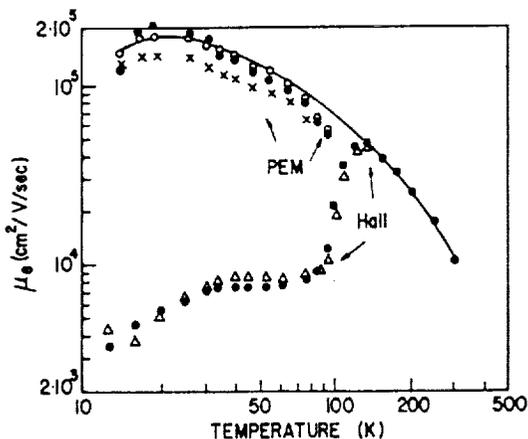


FIG. 2. Electron mobility recorded after the same annealing steps as in Fig. 1. High temperature and low (inversion layer) mobility data is Hall mobility. High mobility at low temperatures (bulk mobility) is derived from PEM experiments. \circ as prepared, \bullet anneal 70°C , Δ 2 days, 80°C , and \times 2 days, 120°C .

that of the inversion electrons. The mobility data is presented in Fig. 2. The high-temperature data and the lower mobilities at lower temperatures are obtained from Hall experiments.

The electron mobility in the inversion layer is very low. Surface scatterings reduce the mobility by more than an order of magnitude. This result is in drastic contrast to the anodic oxide passivation of p -type samples, where we have measured very high electron mobilities, higher than bulk electron mobilities.⁴

The analysis of the PEM data renders the bulk electron mobility. It is interesting to note that this holds true even for the samples with the extensive inversion layers, whose Hall mobilities are considerably lower than those of the bulk. These latter, obtained from the PEM experiments, are practically unchanged by all the heat treatments, and remain almost identical to the as prepared values. Only the final anneal, at 120°C , resulted in a slight deterioration of bulk electron mobility. At 77 K the bulk mobility is typically $9 \times 10^4 \text{ cm}^2/\text{V s}$ which is comparable to electron mobility in n -type material of similar concentration and composition. This is more than twice the mobility in p -type material with concentration of about 10^{16} cm^{-3} .

In the range of 80 – 150 K , the results obtained combine both bulk and inversion layer effects. At extremely low temperatures, i.e., below 30 K , the surface electron mobility decreases further, which is typical of scattering by defects. Again, it indicates that the defect concentration at the surface is much higher than the bulk.

The surface recombination velocity was derived from the PEM data. Following our previous analysis (Equation 7, Ref. 3), the results shown in Fig. 3 are presented as ST/p_0 versus $1/T$, where S is the surface recombination velocity, p_0 is the bulk equilibrium hole concentration and T is the absolute temperature. The present results are compared to those obtained from samples with anodic sulfide passivation of higher bulk concentration p -type HgCdTe, with $p_0 = 5 \times 10^{15}$ – $2 \times 10^{16} \text{ cm}^{-3}$ (Ref. 3). We note that all mea-

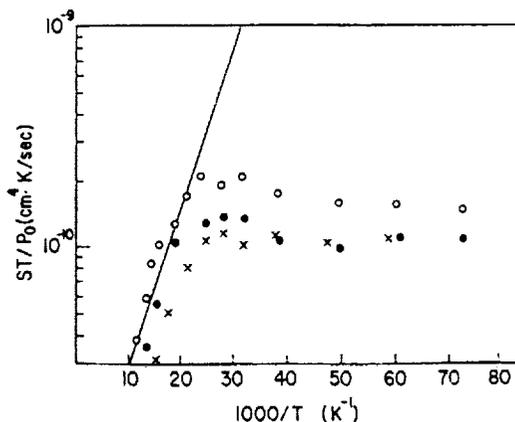


FIG. 3. Surface recombination velocity derived from PEM experiments. Data shows considerable improvement with annealing. Activation energy is 12.5 meV for all cases. \circ as prepared, \bullet anneal 70°C , and \times 2 days, 120°C .

measurements render the same activation energy, of 12.5 meV, which is identical to the energy level of the cation vacancies. Again, there is a low temperature plateau (unlike samples with zinc sulfide treatment), which indicates pinning of the Fermi energy. However, the surface recombination velocity is substantially lower than that obtained with previous samples (with higher bulk concentrations). It improves with annealing, decreasing from about 800 cm/s at 77 K for the as prepared sample to around 250 cm/s following heat treatments. The overall lower recombination with reduced bulk concentration is again indicative of the correlation of the recombination centers to the vacancies in the substrate.

III. CONCLUSIONS

The effect of heat treatment of HgCdTe samples passivated by anodic sulfide was investigated. It was observed that the as prepared samples show very small band bending at the semiconductor interface. The sulfide, however, is produced with internal positive charges, which create an electron image layer at the HgCdTe surface. This electron inversion charge is observed in samples passivated with a thick ($> 100 \text{ \AA}$) sulfide. The surface concentration of these electrons depends on the thickness of the sulfide layer. It is suggested

that the positive charges are evenly distributed in the "as grown" sulfide. A 70–80 °C anneal produces an inversion layer even in materials with a thin sulfide passivation. It is proposed that this layer is the result of migration of positive charges to the interface and their segregation there. The underlying assumption is that the diffusion coefficient is very high, even at these low temperatures. As a result the density of negative image charges in the HgCdTe surface increases. The positive sulfide charges start to anneal at temperatures above 90 °C, thus the inversion layer diminishes. It is shown that while the Hall and conductivity data obtained from inverted *p*-type materials reveal mainly the properties of the high conductivity inversion layers, the parameters extracted from PEM measurements are those of the bulk.

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This work was done while the author was a National Research Council—NASA Research Associate, on leave from the Technion.

²M. B. Reine, A. K. Sood, and T. J. Tredwell, in *Semiconductors and Semimetals*, edited by R. K. Willardson and A. C. Beer (Academic, New York, 1981), Vol. 18, pp. 201–311.

³A. Many, Y. Goldstein, and N. B. Grover, *Semiconductor Surfaces* (North-Holland, Amsterdam, 1965).

⁴E. Finkman and S. E. Schacham, *J. Vac. Sci. Technol. A* 7, 464 (1989).

⁵S. E. Schacham and E. Finkman, *Proc. SPIE* 1106, 206 (1989).